29C318

E1 NIU / ISDN PRI Transceiver

Description

The 29C318 is the first fully integrated transceiver for E1 NIU and ISDN Primary Rate Interface (ISDN PRI) applications at 2.048 MHz. This transceiver operates over 2 km of 0.4 mm twisted-pair cable without any external components.

The 29C318 offers selectable HDB3 encoding/ decoding, and unipolar or bipolar data I/O. The 29C318 also provides jitter attenuation in either the transmit or receive direction starting at 6 Hz, and incorporates a serial interface (SIO) for microprocessor control.

The 29C318 offers a variety of diagnostic features including loopbacks and loss of signal monitoring. It is built using an advanced double-poly, double-metal CMOS process and requires only a single 5-volt power supply.

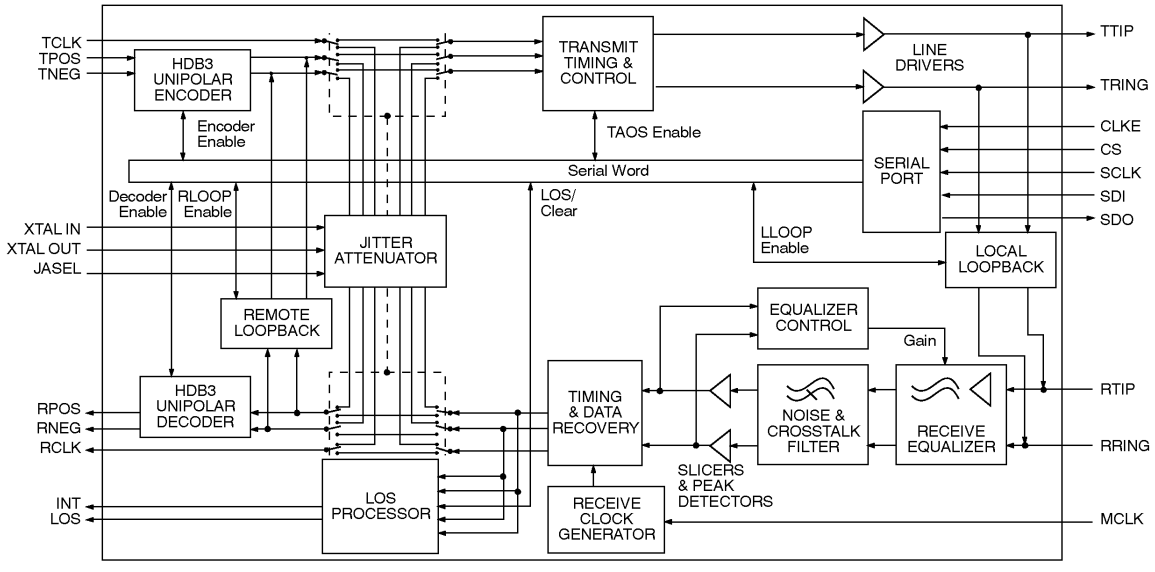
The MHS 29C318 finds applications in widely diverse areas of telecommunication, including

- ISDN Primary Rate Interface (PRI) (CCITT G.703)
- NIU interface to E1 Service
- E1 LAN bridge
- CPU to CPU Channel Extenders
- Digital Loop Carrier - Subscriber Carrier Systems
- E1 Mux
- Channel Banks

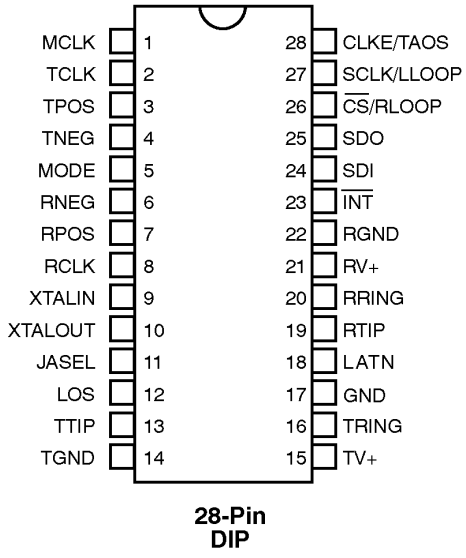
Features

- Fully integrated transceiver comprising : on-chip equalizer ; timing recovery/control ; data processor ; receiver ; transmitter and digital control
- Meets or exceeds CCITT specifications including G.703, G.823
- Fully restores the received signal after transmission through a cable with attenuation of 43 dB @ 1024 kHz
- Selectable unipolar or bipolar data I/O
- Selectable HDB3 encoding/decoding
- Line attenuation indication output
- 138 UI jitter tolerance at 1 Hz
- Output short circuit current limit protection
- On-line idle mode for redundant systems or for testing
- Local, remote and inband network loopback functions
- Receive monitor with loss of signal (LOS) output
- Jitter attenuation starting At 6 Hz, switchable to transmit or receive path (only)
- Microprocessor controllable
- Pin compatible with the 29C310 T1 CSU/ISDN PRI transceiver (1.544 MHz)

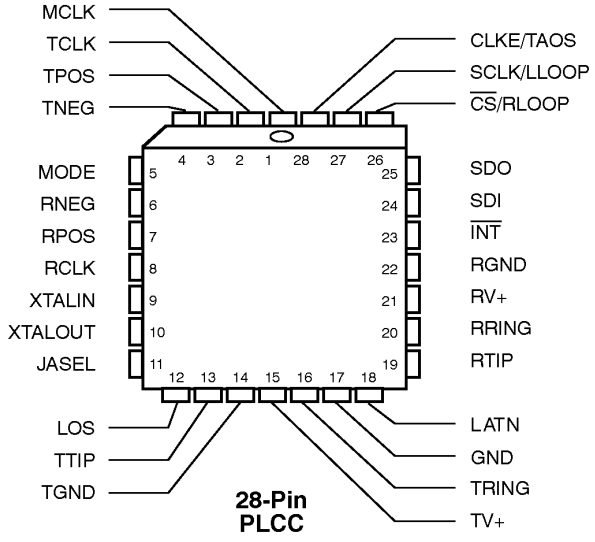
Block Diagram



Interface



28-Pin DIP



28-Pin PLCC

Table 1 : Pin Description

Symbol	Pin #	I/O	Name	Description
MCLK	1	I	Master Clock	A 2.048 MHz clock input used to generate internal clocks. Upon Loss of Signal (LOS), RCLK is derived from MCLK. If MCLK is not applied, this pin should be grounded.
TCLK	2	I	Transmit Clock	Transmit clock input. TPOS and TNEG are sampled on the falling edge of TCLK.
TPOS/ TDATA	3	I	Transmit Data Input	Input for data to be transmitted on the twisted-pair line. Normally, pin 3 is TPOS and pin 4 is TNEG, the positive and negative sides of a bipolar input pair. However, when pin 4 is held high for at least 16 TCLK cycles (equivalent to 15 successive bipolar violations), the 29C318 switches to a unipolar mode. Unipolar mode pin functions are listed in Table 2.
TNEG/ UBS	4	I	Data Input/ Polarity Select	
MODE	5	I	Mode Select	Setting MODE to logic 1 puts the 29C318 in the Host mode. In the Host mode, the serial interface is used to control the 29C318 and determine its status. Setting MODE to logic 0 puts the 29C318 in the Hardware (H/W) mode. In the Hardware mode the serial interface is disabled and hard-wired pins are used to control configuration and report status. Tying MODE to RCLK activates the Hardware mode and enables the HDB3 encoder/decoder.
RNEG/ BPV	6	O	Receive Negative Data	Bipolar data outputs. A signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP/RRING. RNEG/RPOS outputs are Non-Return-to-Zero (NRZ). In Host mode, CLKE determines the clock edge at which these outputs are stable and valid. In Hardware mode both outputs are stable and valid on the rising edge of RCLK. In Unipolar mode, pin 6 output is a Bipolar Violation indication and pin 7 is the unipolar data output. See Table 2 for Unipolar mode functions.
RPOS/ RDATA	7	O	Receive Positive Data	
RCLK	8	O	Receive Clock	This is the clock recovered from the signal received at RTIP and RRING.
XTALIN	9	I	Crystal Input	An external crystal (18.7 pF load capacitance, pullable) operating at four times the bit rate (8.192 Mhz) is required to enable the jitter attenuation function of the 29C318. These pins may also be used to disable the jitter attenuator by connecting the XTALIN pin to the positive supply through a resistor, and tying the XTALOUT pin to ground.
XTALOUT	10	O	Crystal Output	
JASEL	11	I	Jitter Attenuation Select	Selects jitter attenuation location. When JASEL = 1, the jitter attenuator is active in the receive path. When JASEL = 0, the jitter attenuator is active in the transmit path.
LOS	12	O	Loss Of Signal	LOS goes to a logic 1 when 175 consecutive spaces have been detected. LOS returns to a logic 0 when the received signal reaches a mark density of 12.5 % (determined by receipt of four marks within 32 bit periods.) Received marks are output on RPOS and RNEG even when LOS is at logic 1.
TTIP	13	O	Transmit Tip	Differential Driver Outputs. These outputs are designed to drive a 50 - 200 Ω load. Line matching resistors and transformer can be selected to give the desired pulse height.
TRING	16	O	Transmit Ring	
TGND	14	-	Tx Ground	Ground return for the transmit drivers power supply TV+.
TV+	15	I	Transmit Power Supply	+ 5 VDC power supply input for the transmit drivers. TV+ must not vary from RV+ by more than ± 0.3 V.
GND	17		Ground	
LATN	18	O	Line Attenuation Indication	Encoded output. Pulse width, relative to RCLK, indicates receive equalizer gain setting (line insertion loss at 1024 kHz) in 9.5 dB steps. When LATN = 1 RCLK pulse, the equalizer is set at 9.5 dB gain ; 2 pulses = 19 dB ; 3 pulses = 28.5 dB and 4 pulses = 0 dB. Output is valid on the rising edge of RCLK.

Table 1 : Pin Description (continued)

Symbol	Pin #	I/O	Name	Description
RTIP	19		Receive Tip	The AMI signal received from the line is applied at these pins. A 1:1 transformer is required. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG, and RCLK pins.
RRING	20	|	Receive Ring	
RV+	21	I	Receive Power Supply	+ 5 VDC power supply for all circuits except the transmit drivers. (Transmit drivers are supplied by TV+.)
RGND	22	-	Rx Ground	Ground return for power supply RV+.
INT	23	O	Interrupt	In Host mode, this 29C318 output goes low to flag the host processor when LOS changes state. INT is an open drain output and should be tied to power supply RV+ through a resistor. INT is reset by clearing the LOS register bit. In hardware mode this pin is inactive and should be tied to ground.
SDI	24	I	Serial Data In *(Host Mode)*	The serial data input stream is applied to this pin when the 29C318 operates in the Host mode. SDI is sampled on the rising edge of SCLK. In Hardware mode this pin is inactive and should be tied to ground.
SDO	25	O	Serial Data Out *(Host Mode)*	The serial data from the on-chip register is output on this pin in the 29C318 Host mode. If CLKE is high, SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to. This pin is inactive in hardware mode and should be tied to ground.
$\overline{CS}$	26	I	Chip select *(Host Mode)*	This input is used to access the serial interface in the 29C318 Host mode. For each read or write operation, $\overline{CS}$ must transition from high to low, and remain low.
RLOOP		I	Remote Loopback *(H/W Mode)*	This input controls loopback in the 29C318 Hardware mode. Setting RLOOP to a logic 1 enables Remote Loopback. During Remote Loopback, in-line encoders and decoders are bypassed. Setting both RLOOP and LLOOP while holding TAOS low causes a Reset.
SCLK	27	I	Serial Clock *(Host Mode)*	This clock is used in the 29C318 Host mode to write data to or read data from the serial interface registers.
LLOOP		I	Local Loopback *(H/W Mode)*	This input controls loopback functions in the 29C318 Hardware mode. Setting LLOOP to a logic 1 enables the Local Loopback Mode. Setting both LLOOP and RLOOP while holding TAOS low causes a Reset.
CLKE	28	I	Clock Edge *(Host Mode)*	Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. When CLKE is a logic 0, RPOS and RNEG are valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK.
TAOS		I	Transmit All Ones *(H/W Mode)*	When set to a logic 1, TAOS causes the 29C318 Hardware mode to transmit a continuous stream of marks at the TCLK frequency. Activating TAOS causes TPOS and TNEG inputs to be ignored. TAOS is inhibited during Remote Loopback.

Functional Description

The 29C318 is fully integrated PCM transceiver for 2.048 MHz (E1) applications. It allows full-duplex transmission of digital data over existing twisted-pair installations.

The 29C318 transceiver interfaces with two twisted-pair lines (one twisted-pair for transmit, one twisted-pair for receive) through standard pulse transformers and appropriate resistors.

Figure 1 is a block diagram of the 29C318. This transceiver may be controlled by a microprocessor through the serial port (Host Mode), or by individual pin settings (Hardware Mode). The jitter attenuator may be positioned in either the transmit or receive path.

Table 2 : Unipolar Data I/O Pin Description

Symbol	Pin #	I/O	Name	Description
TDATA	3	I	Transmit Data Input	Unipolar input for data to be transmitted on the twisted-pair line.
UBS	4	I	Uni-Bi Polarity Select	When pin 4 is held high for at least 16 TCLK cycles (equivalent to 15 successive bipolar violations), the 29C318 switches to unipolar data I/O. The device immediately returns to bipolar I/O when pin 4 goes low.
BPV	6	O	Bipolar Violation	Pin 6 goes high when a bipolar violation is received.
RDATA	7	O	Receive Data	Unipolar data output. RDATA is a Non-Return-to-Zero (NRZ) output. In Host mode, CLKE determines the clock edge at which RDATA is stable and valid. In Hardware mode RDATA is stable and valid on the rising edge of RCLK.

Note : Table 2 lists only those pins which are affected by the switch to unipolar data I/O.

Transmitter

Input data (bipolar or unipolar) for transmission onto the line is clocked serially into the device. Bipolar data input at pin 3 (TPOS) and pin 4 (TNEG). Unipolar data is input at pin 3 (TDATA) only. (Unipolar mode is enabled by holding pin 4 high for 16 RCLK cycles). Input data may be passed through the Jitter Attenuator and/or HDB3 encoder, if selected. In Host mode, HDB3 is selected by setting bit D3 of the input data byte. In Hardware mode, HDB3 is selected by connecting the MODE pin to RCLK. Input synchronization is supplied by the transmit clock (TCLK). Timing requirements for TCLK and the Master Clock (MCLK) are defined in Table 3 and Figure 2.

Idle Mode

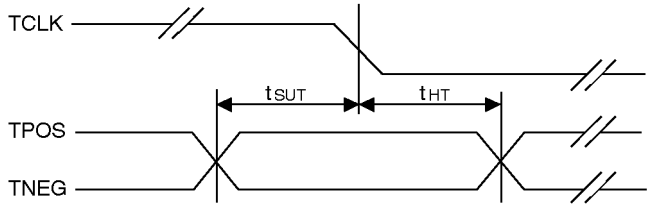
The 29C318 incorporates a transmit idle mode. This allows multiple transceivers to be connected to a single line for redundant applications or for testing purposes. TTIP and TRING remain in a high impedance state when TCLK is not present (TCLK grounded). The high impedance state can be temporarily disabled by enabling Remote Loopback.

Table 3 : 29C318 Master Clock and Transmit Timing Characteristics (See Figure 2)

Symbol	Parameter	Min	Typ[1]	Max	Units	Notes
MCLK	Master clock frequency	-	2.048	-	MHz	
MCLKt	Master clock tolerance	-	± 100	-	ppm	
MCLKd	Master clock duty cycle	40	-	60	%	
fc	Crystal frequency	-	8.192	-	MHz	
TCLK	Transmit clock frequency	-	2.048	-	MHz	
TCLKt	Transmit clock tolerance	-	-	± 100	ppm	
TCLKd	Transmit clock duty cycle	10	-	90	%	
t_{SUT}	TPOS/TNEG to TCLK setup time	50	-	-	ns	
t_{HT}	TCLK to TPOS/TNEG Hold time	50	-	-	ns	

Note : 1. Typical figures are at 25 °C and are for design aid only ; not guaranteed and not subject to production testing.

Figure 2. 29C318 Transmit Clock Timing



Short Circuit Limit

The 29C318 transmitter is equipped with a short-circuit limiter. This feature limits to approximately 120 mA RMS the current the transmitter will source into a low-impedance load. The limiter trips when the RMS current exceeds the limit for 100 µs (~ 150 marks). It automatically resets when the load current drops below the limit.

The 29C318 meets or exceeds CCITT specifications for NIU applications, as well requirements for ISDN PRI.

Line Code

The 29C318 transmits data as a 50 % AMI line code as shown in Figure 3. Power consumption is reduced by activating the AMI line driver only to transmit a mark. The output driver is disabled during transmission of a space. Biasing of the transmit DC level is on-chip.

Shaped pulses meeting the various CCITT requirements and ISDN PRI requirements are applied to the AMI line driver for transmission onto the line at TTIP and TRING. Refer to Figure 4 for E1 pulse mask specifications.

Receiver

The receiver input from the twisted-pair is received through a 1:1 transformer. Recovered data is output at RPOS/RNEG (RDATA in Unipolar mode), and recovered clock is output at RCLK. Refer figure 5.

The signal received at RTIP and RRING is processed through the receive equalizer which may apply of to 43 dB of gain. Insertion loss of the line, as indicated by the receive equalizer setting, is encoded in the LATN output as shown Figure 5a.

Figure 3. 50 % Ami Coding Diagram

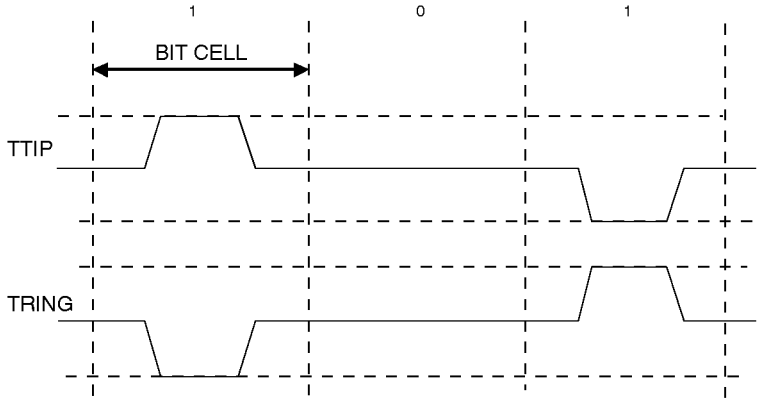
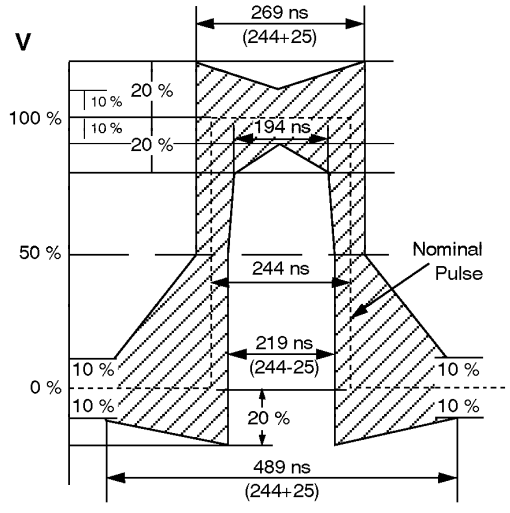


Figure 4. 2.048 MHz E1 Pulse Mask



Parameter	COAX	Shielded TP	Units
Test load impedance	75	120	Ω
Nominal peak mark voltage	2.37	3.0	V
Nominal peak space voltage	0 ± 0.237	0 ± 0.30	V
Nominal pulse width	244	244	ns
Ratio of positive and negative pulse amplitudes at center of pulse	95-105	95-105	%
Ratio of positive and negative pulse amplitudes at nominal half amplitude	95-105	95-105	%

Table 4 : 29C318 Receive Timing Characteristics. (See Figure 5)

Symbol	Parameter	Min	Typ[1]	Max	Units
RCLKd	Receive clock duty cycle[2]	40	50	60	%
t_{PW}	Receive clock pulse width[2]	-	488	-	ns
t_{PWH}	Receive clock pulse width high	-	244	-	ns
t_{PWL}	Receive clock pulse width low	220	244	268	ns
t_{SUR}	RPOS/RNEG to RCLK rising setup time	-	194	-	ns
t_{HR}	RCLK rising to RPOS/RNEG hold time	-	194	-	ns

Notes :
1. Typical figures are at 25 °C and are for design aid only ; not guaranteed and not subject to production testing.
2. RCLK duty cycle widths will vary depending on extent of received pulse jitter displacement. Max and Min RCLK duty cycles are for worst case jitter conditions (0.4 UI clock displacement for 2.048 MHz).

Figure 5. 29C318 Receive Clock Timing

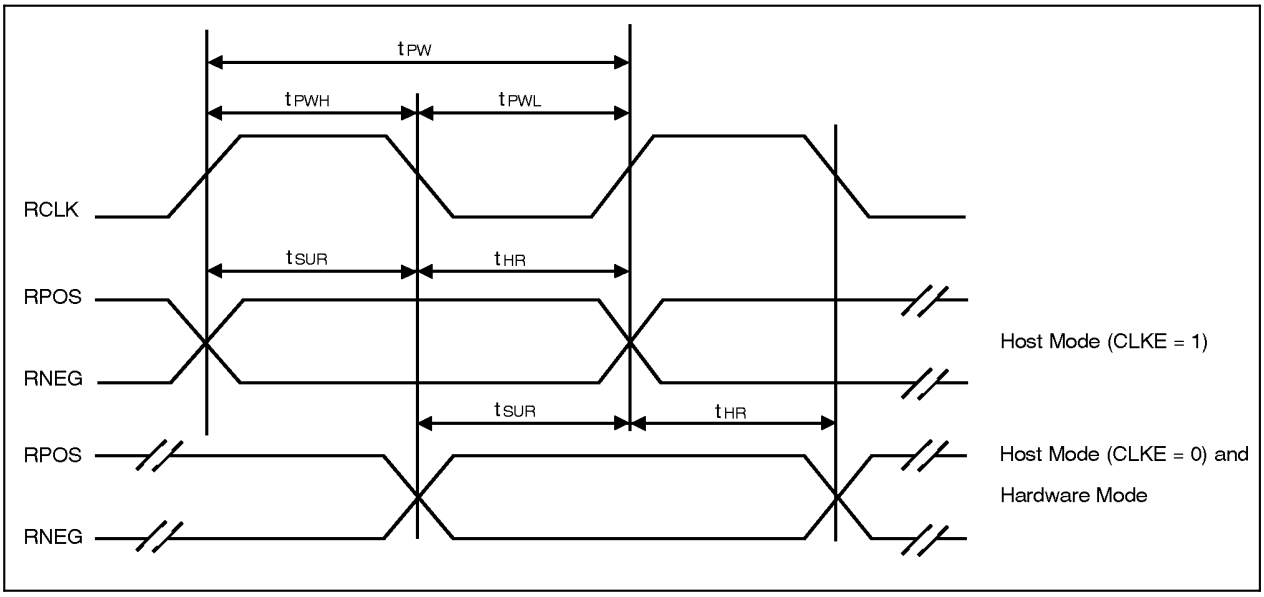
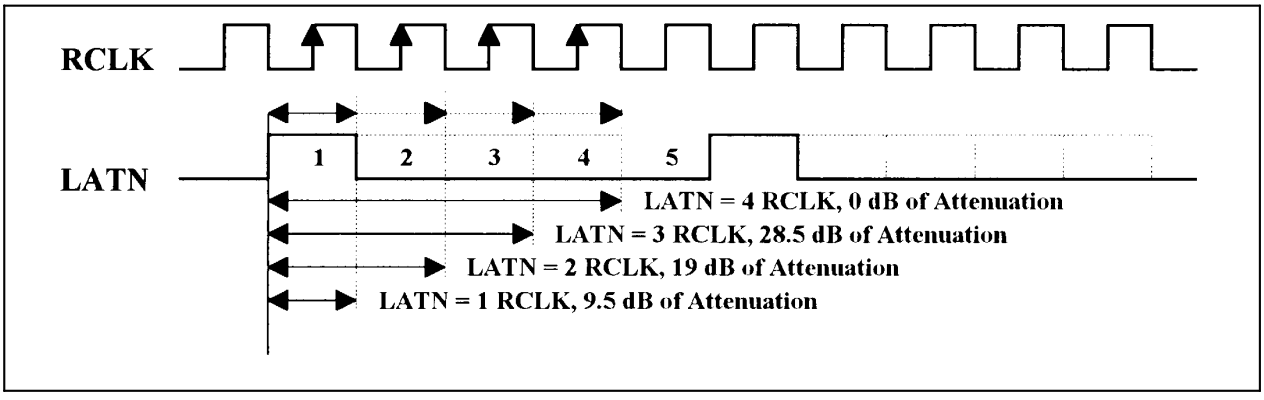


Figure 5a. LATN Pulse Width Encoding



The equalized signal is filtered and applied to the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided of the data slicers as a threshold level to ensure optimum signal-to-noise ratio. The threshold is set to 50 % of the peak value. The receiver is capable of accurately recovering signals with up to 43 dB of cable attenuation (from 2.7 V).

After processing through the data slicers, the received signal is routed to the data and timing recovery section, then to the HDB3 decoder (if selected) and to the LOS processor. The LOS Processor loads a digital counter at the RCLK frequency. The count is incremented each time a zero (space) is received, and reset to zero each time a one (mark) is received. Upon receipt of 175 consecutive zeros the LOS pin goes high, and a smooth transition replaces the RCLK output with the MCLK. (*During LOS, if MCLK is not supplied and JASEL = 1, the RCLK output is replaced with the centered crystal clock.)*

Received marks will be output regardless of the LOS status, but the LOS pin will not reset until the ones density reaches 12,5 %. This level is based on receipt of at least 4 ones in any 32 bit periods.

Jitter Attenuation

Jitter attenuation, is provided by a Jitter Attenuation Loop (JAL) and an Elastic Store (ES). An external crystal oscillating at 4 times the bit rate provides clock stabilization. Refer to Table 5 for crystal specifications. The

ES is a 32 × 2-bit register. When JASEL = 1, the JAL is positioned in the receive path. When JASEL = 0, the JAL is positioned in the transmit path.

Data (TPOS/TNEG/TDATA or RPOS/RNEG/ RDATA) is clocked into the ES with the associated clock signal (TCLK or RCLK), and clocked out of the ES with the dejittered clock from the JAL. When the bit count in the ES is within two bits of overflowing or underflowing, the ES adjusts the output clock by 1/8 of a bit period. The ES produces an average delay of 16 bits in the associated path.

Operating Modes

The 29C318 can be controlled by a microprocessor through a serial interface (Host mode), or through individual hard-wired pins (Hardware mode). The mode operation is selected by the MODE pin logic level. With MODE pin set to 1, the 29C318 operates in Host mode. With Mode pin set to 0, the 29C318 operates in Hardware mode. With MODE tied to RCLK, the 29C318 operates in Hardware mode with HDB3 encoder/decoder enabled.

Table 5 : Crystal Specifications (External)

Parameter	Specification
Frequency	8.192 MHz
Frequency Stability	± 20 ppm @ 55 °C
	± 25 ppm from - 40 °C to + 85 °C
	(Ref 25 °C reading)
Pullability	CL = 11 pF to 18.7 pF, +ΔF = 175 to 195 ppm
	CL = 18.7 pF to 34 pF, -ΔF = 175 to 195 ppm
Effective series resistance	40 Ω Maximum
Crystal cut	AT
Resonance	Parallel
Maximum drive level	2.0 mW
Mode of operation	Fundamental
Crystal holder	HC49 (R3W), C_o = 7 pF maximum C_M = 17 fF typical

Table 6 : 29C318 Serial Data Output Bit Coding (See Figure 6)

Bit D5	Bit D6	Bit D7	Status
0	0	0	Reset has occurred, or no program input
0	0	1	TAOS active
0	1	0	LLOOP active
0	1	1	TAOS and LLOOP active
1	0	0	RLOOP active
1	0	1	Reserved
1	1	0	LOS has changed state since last Clear LOS occurred
1	1	1	Reserved

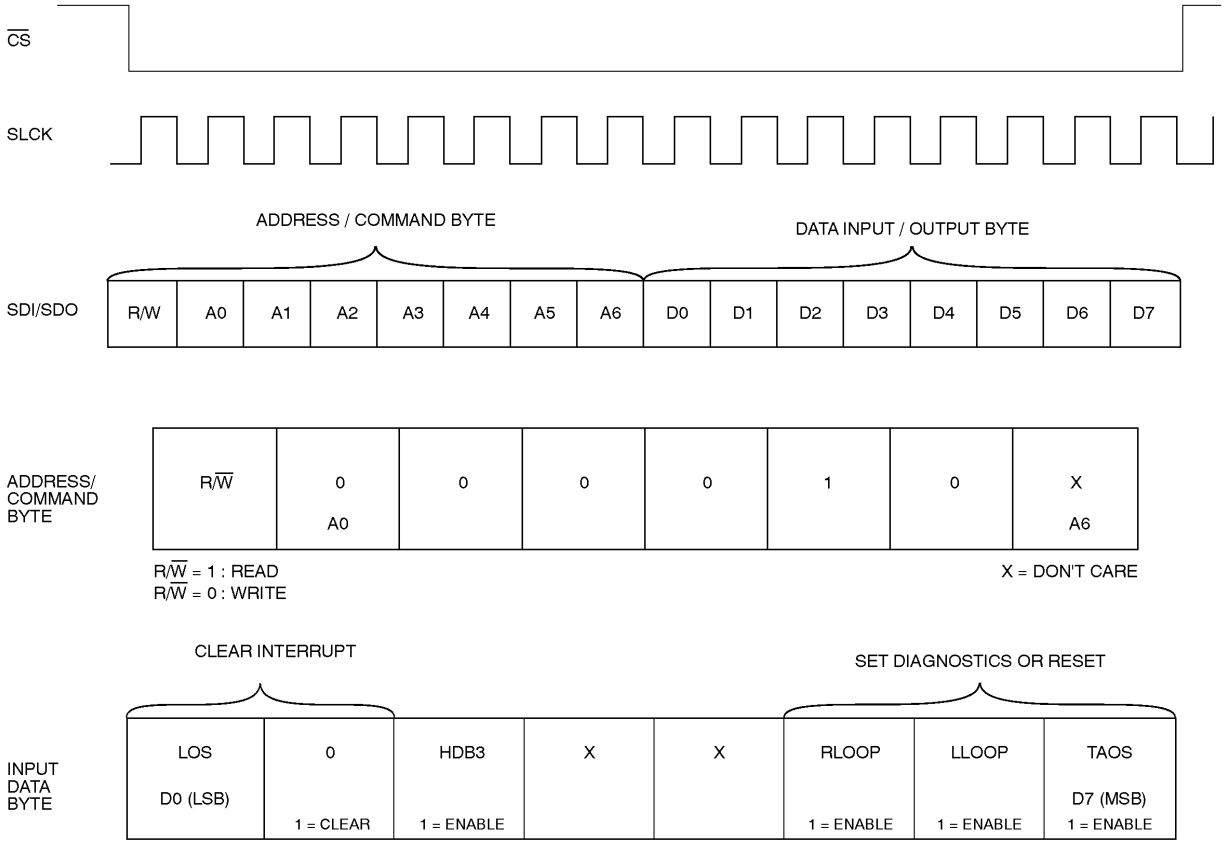
Host Mode Operation

The 29C318 operates in the Host mode when MODE is set to 1. The 16-bit serial word consists of an 8-bit Command/Address byte and an 8-bit Data byte. Table 6 lists the output data bit combinations. Figure 6 shows the serial interface data structure and timing. The Host mode provides a latched Interrupt output (INT) which is triggered by a change in the LOS bit. The Interrupt is cleared when the interrupt condition no longer exists, and the host processor writes a one to the respective bit in the serial input data byte. Host mode also allows control of the serial data and receive data output timing. The Clock Edge (CLKE) signal determines when the outputs are valid, relative to the Serial Clock (SCLK) or RCLK as listed in Table 7.

Table 7 : CLKE Settings

CLKE	Output	Clock	Valid Edge
LOW	RPOS RNEG SDO	RCLK RCLK SCLK	Rising Rising Falling
HIGH	RPOS RNEG SDO	RCLK RCLK SCLK	Falling Falling Rising

Figure 6. 29C318 Serial Interface Data Structure



Note : Output data Byte same as Input data byte shown above, except for bits D5 through D7 listed in table 6.

The 29C318 serial port is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. The 29C318 contains only a single output data register so no complex chip addressing scheme is required. The register is accessed by causing the Chip Select (CS) input to transition from high to low. Bit 1 of the serial Address/Command byte provides Read/Write control when the chip is accessed. A logic 1 indicates a read operation, and a logic 0 indicates a write operation. Serial data I/O timing characteristics are shown in Table 8, and figures 7 and 8.

Hardware Mode Operation

In Hardware mode the transceiver is accessed and controlled through individual pins. With the exception of the INT and CLKE functions, Hardware mode provides all the functions provided in the Host mode. In the Hardware mode RPOS/RNEG or RDATA outputs are valid on the rising edge of RCLK. The 29C318 operates in Hardware mode only when MODE is set to 0 or connected to RCLK.

Initialization and Reset Operation

Upon power up, the transceiver is held static until the power supply reaches approximately 3 V. Upon crossing this threshold, the device begins a 32 ms reset cycle to calibrate the transmit and receive delay lines and lock the Phase Lock Loop to the receive line. A reference clock is required to calibrate the delay lines. The transmitter reference is provided by TCLK.

The crystal oscillator provides the receiver reference. If the crystal oscillator is grounded, MCLK is used as the receiver reference clock.

The transceiver can also be reset from the Host or Hardware mode. In Host mode, reset is commanded by simultaneously writing ones to RLOOP and LLOOP, and a zero to TAOS. In Hardware mode, reset is commanded by holding RLOOP and LLOOP high simultaneously for 200 ns while holding TAOS low. In either mode, reset clears and sets all registers to 0.

Diagnostic Mode Operation

In Transmit All Ones (TAOS) mode the TPOS and TNEG inputs to the transceiver are ignored and the transceiver transmits a continuous stream of 1’s at the TCLK frequency. (In the 29C318 with JASEL = 0 and TCLK not provided, TAOS is locked to the MCLK.) This can be used as the Blue Alarm Indicator (AIS). In Host mode, TAOS is commanded by writing a one to bit D7 of the input data byte. In Hardware mode, TAOS is commanded by setting pin 28 high. TAOS can be commanded simultaneously with Local Loopback, but is inhibited during Remote Loopback.

Local Loopback (LLOOP) is designed to exercize the maximum number of functional blocks. During LLOOP operation, the RTIP/RRING inputs from the line are disconnected. Instead, the transmit outputs are routed back into the receive inputs. This tests the encoders/decoders, jitter attenuator, transmitter, receiver and timing recovery sections. In Host mode, Local Loopback is commanded by writing a one to bit D6 of the input data byte. In Hardware mode, Local Loopback is commanded by setting pin 27 high. If TAOS and NLOOP are both set, the All Ones pattern is transmitted onto the line while the TPOS/TNEG input data is looped back to the RPOS/RNEG outputs.

In Remote Loopback (RLOOP) mode, the transmit data and clock inputs (TCLK and TPOS/TNEG or TDATA) are ignored, and the in-line encoders and decoders are bypassed. The RPOS/RNEG or RDATA outputs are looped back through the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the RCLK and RPOS/RNEG or RDATA signals received from the twisted-pair line. In Host mode, Remote Loopback is commanded by writing a one to bit D5 of the input data byte. In Hardware mode, Remote Loopback is commanded by setting pin 26 high.

Application Considerations

Power Requirements

The 29C318 is low-power CMOS devices. It operates from a single +5 V power supply which can be connected externally to both the transmitter and receiver. However, the two inputs must be within ±.3 V of each other, and decoupled to their respective grounds separately. Isolation between the transmit and receive circuits is provided internally.

The line attenuation (LATN) output is encode as a simple serial bit stream for use in monitoring applications. The table below provides the decode output for each equalizer setting. The decoder can be realised with a 2-bit synchronous counter with a synchronous reset, and a pair or flip-flop.

L1	L2	Line Attenuation
0	0	0.0 dB
0	1	–9.5 dB
1	0	–19.0 dB
1	1	–28.5 dB

Table 8 : 29C318 Serial I/O Timing Characteristics (See Figures 7 and 8)

PARAMETER	SYM	MIN	TYP[1]	MAX	UNITS	TEST CONDITIONS
Rise/Fall time - any digital output	t_{RF}	-	-	100	ns	Load 1.6 mA, 50 pF
SDI to SCLK setup time	t_{DC}	50	-	-	ns	
SCLK to SDI hold time	t_{CDH}	50	-	-	ns	
SCLK low time	t_{CL}	240	-	-	ns	
SCLK high time	t_{CH}	240	-	-	ns	
SCLK rise and fall time	t_R, t_F	-	-	50	ns	
CS to SCLK setup time	t_{CC}	50	-	-	ns	
SCLK to CS hold time	t_{CCH}	50	-	-	ns	
CS inactive time	t_{CWH}	250	-	-	ns	
SCLK to SDO valid	t_{CDV}	-	-	200	ns	
SCLK falling edge or CS rising edge to SDO high Z	t_{CDZ}	-	100	-	ns	
Note : 1. Typical figures are at 25 °C and are for design aid only ; not guaranteed and not subject to production testing						

Figure 7. 29C318 Serial Data Input Timing Diagram

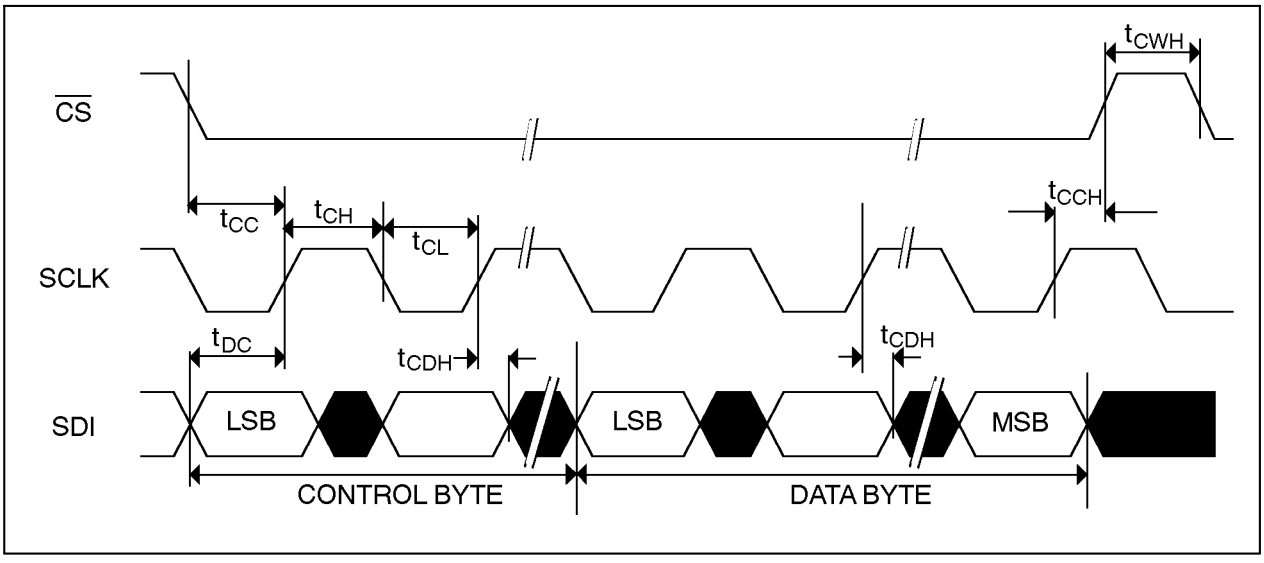


Figure 8. 29C318 Serial Data Output Timing Diagram

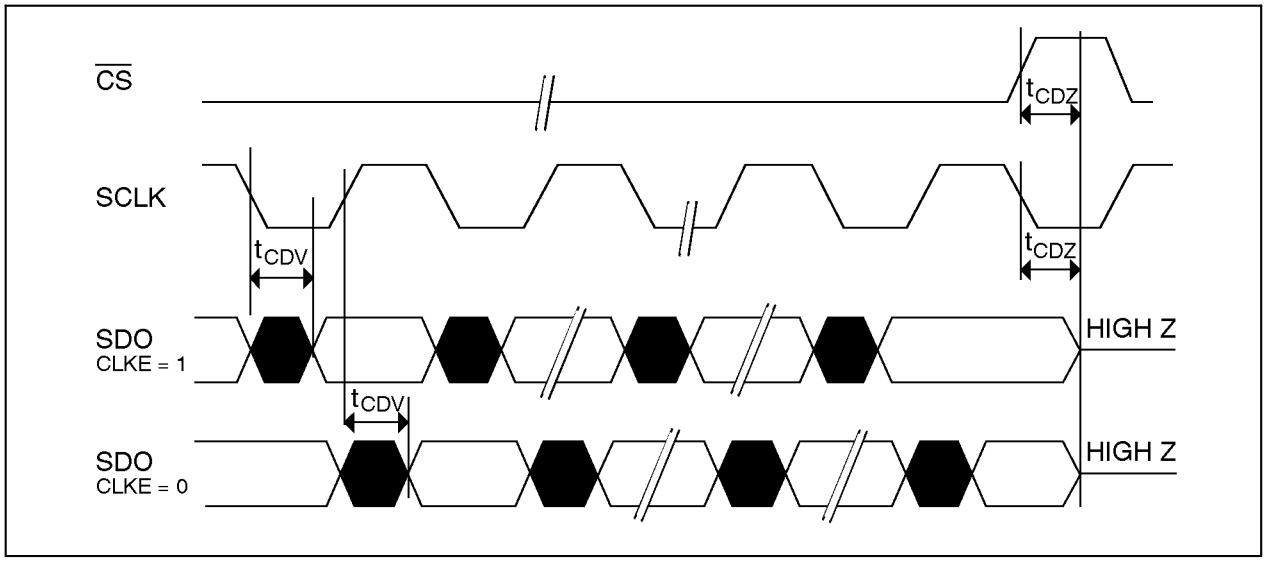


Table 9 : Approved Crystals and Transformers

Component	Manufacturer	Part Nnmbers
Crystal (8.192 MHz)	M-Tron Monitor Products CTS Knights Valpey Fisher U.S. Crystal	MP-1-8192 MSC1311-01B-8.192 8192-100 VF49A16FN1-8.192 U18-18-8192SP
Tx Transformer (1:2)	Pulse Engineering Bell Fuse Midcom Schott Corp	65351 0553-5006-IC 671-5832 67112060 and 67115100
Rx Transformer (1:1)	Schott Corp Midcom Pulse Engineering	67109510 671-5792 64936 and 65400

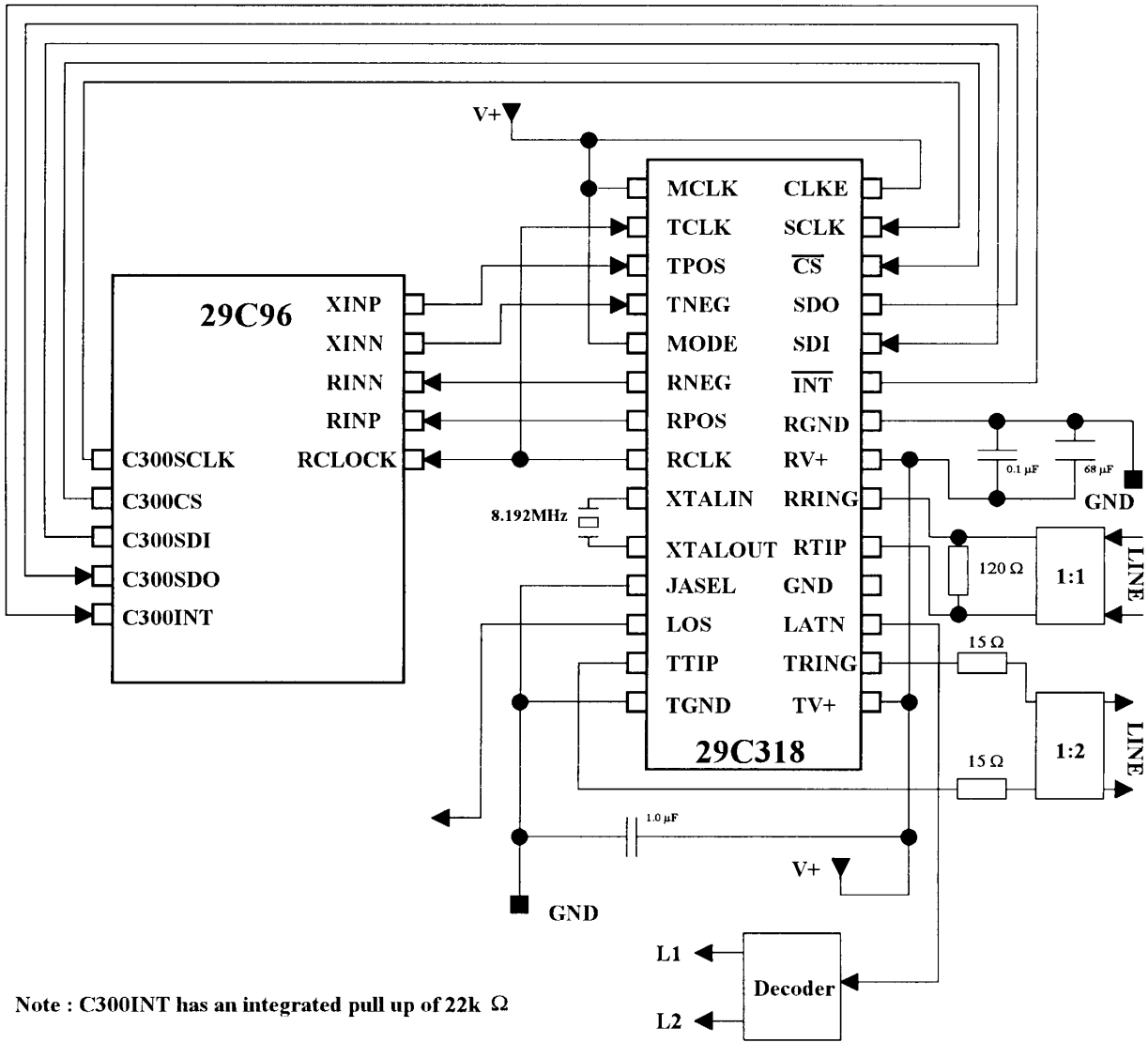
29C318 Host Mode Applications

Figure 9 shows a typical E1 NIU application with the 29C318 operating in the Host mode (MODE pin tied high). The 29C96 E1 CRC Framer provides the digital interface with the host controller. The 29C318 Serial Interface can be directly connected to the 29C96 serial interface, the 29C318 will thus be controlled by a local CPU thru the 29C96 with no extra hardware. In the Host mode, the LOS alarm is reported via the serial port so the LOS pin is allowed to float.

The 8.192 MHz crystal across XTALIN and XTALOUT enables the JAL which is switched to the transmit side by the ground on JASEL. (Refer to Table 9 for approved crystals and transformers.) The power supply inputs are tied to a common bus with appropriate decoupling capacitors (68 µF and 0.1 µF) installed on each side.

The twisted-pair interfaces are relatively simple. A 120 Ω resistor across the input of a 1:1 transformer is used on the receive side, and a pair of 12.5 Ω resistors are installed in line with the 1:2 output transformer.

Figure 9. Typical 29C318 Host Mode E1/NIU Application. The 29C96 can be connected with the 29C318 through a serial interface.

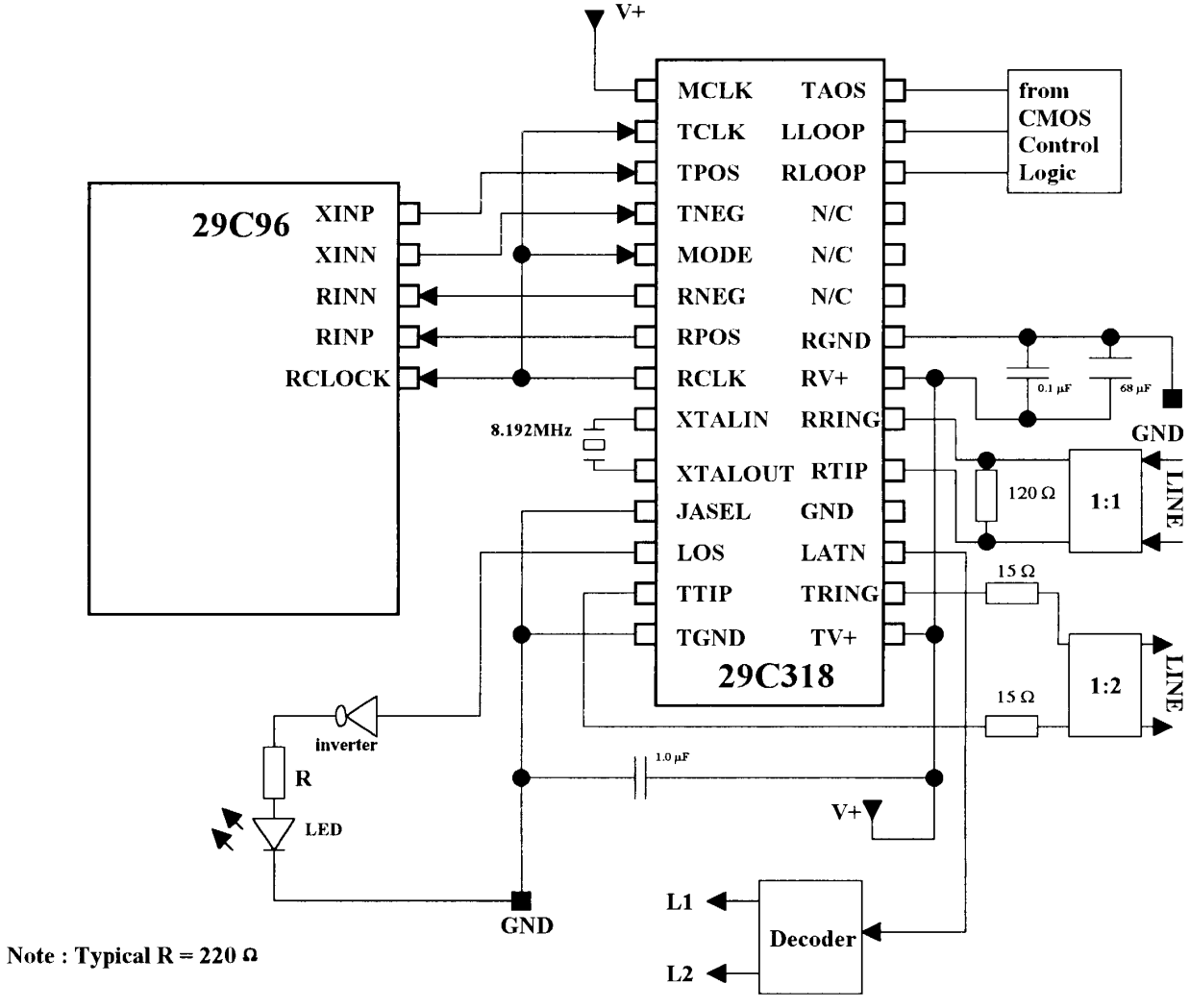


Note : C300INT has an integrated pull up of 22k Ω

29C318 Hardware Mode Applications

Figure 10 is a typical 2.048 MHz ISDN PRI application with the 29C318 operating in the Hardware mode with the 29C96 Framer. As in the E1 NIU application Figure 9, this configuration is illustrated with a single power supply bus. The CMOS logic is used to set TAOS, LLOOP and RLOOP diagnostic modes individually. The RCLK input to the OR gate at RLOOP allows for clocking of the RLOOP pin, which enables HDB3 encoding. The receive and transmit line interfaces are identical to the Host mode application shown in Figure 9.

Figure 10. Typical 29C318 Hardware Mode Application. The 29C96 can be connected with the 29C318 through a serial interface.



Electrical Characteristics

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
RV+, TV+	DC supply (referenced to GND)	-	6.0	V
V_{IN}	Input voltage, any pin	RGND - 0.3	RV+ + 0.3	V
I_{IN}	Input current, any pin[1]	- 10	10	mA
T_A	Ambient operating temperature	- 40	85	°C
T_{STG}	Storage temperature	- 65	150	°C

WARNING : Operations at or beyong these limits may result in permanent damages to the device. Normal operation not guaranteed at these extremes.

Note 1 : Transient currents of up to 100 mA will not cause SCR latch-up. TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

Operating Conditions/Characteristics

Symbol	Parameter	Min	Typ [1]	Max	Units	Test Conditions
RV+ TV+	DC[2] supply	4.75	5.0	5.25	V	
T_A	Ambient operating temperature	–40		85	°C	
P_D	Power dissipation[3]	-	300	400	mW	100 % ones density & maximum line length

Notes :
1. Typical figures are at 25°C and are for design aid only ; not guaranteed and not subjecto to production testing.
2. TV+ must not exceed RV+ by more than 0.3 V.
3. Power dissipation while drinving 25 Ω load over operating temperature range. Includes device and load. Digital input levels are within 10 % of the supply rails and digital outputs are driving a 50 pF capacitive load.

Digital Characteristics (T_A = -40° to 85°C, V+ = 5.0 V ± 5 %, GND = 0 V)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{IH}	High level input voltage [1,2] (pins 1-5, 10, 23-28)	2.0	-	-	V	
V_{IL}	Low level input voltage [1,2] (pins 1-5, 10, 23-28)	-	-	0.8	V	
V_{OH}	High level output voltage [1,2] (pins 6-8, 12, 23, 25)	2.4	-	-	V	I_{OUT} = - 400 µA
V_{OL}	Low level output voltage [1,2] (pins 6-8, 12, 23, 25)	-	-	0.4	V	I_{OUT} = 1.6 mA
I_{LL}	Input leakage current	0	-	± 10	µA	
I_{3L}	Three-state leakage current[1] (pin 25)	0	-	± 10	µA	

Notes :
1. Functionality of pins 23 and 25 depends on mode. See Host/Hardware Mode descriptions.
2. Output drivers will output CMOS logic levels into CMOS loads

Analog Characteristics (T_A = -40°C to 85°C, V+ = 5.0 V ± 5 %, GND = 0 V)

Parameter	Min	Typ[1]	Max	Units	Test Conditions
Recommended output load at TTIP and TRING	50	120	200	Ω	
AMI Output Pulse Amplitudes	2.7	3	3.3	V	
Jitter added by the transmitter[2] 20 Hz – 100 kHz[3]			0.05	UI	Mesured at the output
Input jitter tolerance 20 kHz – 100 kHz 10 Hz	 0.2 100	 0.3 500		 UI UI	0 – 43 dB line
Jitter attenuation curve corner frequency[4]		6		Hz	
Receive signal attenuation range @1024 kHz	0	43		dB	

Notes :
1. Typical figures are at 25°C and are for design aid only ; not guaranteed and not subject to production testing.
2. Input signal to TCLK is jitter-free.
3. Guaranteed by characterization ; not subject to production testing.
4. Circuit attenuates jitter at 20 dB/decade above the corner frequency.

Ordering Information